POLI ESCOLA SUPERIOR TECNOLOGIA GESTÃO TÉCNICO GUARDA	**SUBJECT DESCRIPTION**	**MODELO** PED.013.03

Course	**Computer Science**					
Subject	**Digital Systems II**					
Academic year	2023/2024	*Curricular year*	2nd	*Study period*	1st semester	
Type of subject	Compulsory	*Student workload (H)*	Total: 140	Contact: 105	*ECTS*	5
Professor(s)	António Mário Ribeiro Martins					
☒ *Area/Group Coordinator* ☐ *Head of Department* *(select)*	Fernando Melo Rodrigues					

PLANNED SUBJECT DESCRIPTION

1. LEARNING OBJECTIVES

Upon completion of the UC, students should be able to: Describe latches and flip-flops, describe several types of register and counter design, design sequential arithmetic circuits, explain how memory works: ROM and RAM expansion design, DAC design, explain how some ADC's work, design sequential synchronous systems using Mealy or Moore methods and design simple digital controllers using shift registers.

2. PROGRAMME

SR and D latches. Master slave SR and Jk flip-flop. ´D´ flip-flop positive edge triggered. Sincronous and diret inputs.

Basic registers with control inputs. Shift registers. Registers interconnection and groups of registers. Asynchronous counters. Timing diagrams. Design in a modulus that is not a power of two. Synchronous counters using JK or D flip-flops. Counters as registers.

Sequential arithmetic circuits: Serial and parallel adders. Accumulators, multiplier, divider and BCD to binary conversion.

Digital system design. Mealy and Moore models. State diagrams and state transition tables.

Digital to analogue conversion. The weighted resistance circuit and the R-2R ladder. Analog to digital conversion: Counting, successive approximation, and parallel-convertor types.

Types of memories: ROM and RAM. The decoded ROM, and static RAM basic cell. Expansion problems.

Controller design using shift registers.

3. COHERENCE BETWEEN PROGRAMME AND OBJECTIVES

Register and counter design, must be preceded by the study of latches and flip-flops. The operation of sequential arithmetic circuits is taught as well. For the synchronous digital systems

design, it is necessary to teach Mealy and Moore models, state diagrams and state transition tables, and state diagrams simplified by eliminating redundant states. Regarding DAC and ADC design, this will only be possible if the respective circuits are taught to students.

For the pedagogical purpose of explaining memories design, the professor explain ROM and RAM internal circuits. Project using shift register is also considered.

4. MAIN BIBLIOGRAPHY

Mandatory:

Arroz et all, Arquitetura de Computadores e circuitos digitais, IST PRESS, 2008

Pedro Guedes de Oliveira e Dinis Magalhães Santos, Electrónica, Uma Visão de Projeto, U.Porto Edições july 2018.

Taub, H. & Schilling, D. (1977), *Digital Integrated Electronics*, McGraw Hill.

Ferreira, J.M. (1998), *Introdução ao Projecto com Sistemas Digitais e Microcontroladores*, FEUP.

Sandige R., Modern Digital Design, McGraw-Hill

5. TEACHING METHODOLOGIES (INCLUDING EVALUATION)

a. Teaching methodologies:

Lecture

Interactive lesson

Problem solving

Lab work

b. Evaluation methodologies:

Continuous evaluation, with 2 tests and normal examination, weights 70%, with minimal mark of 6. Two Lab works (30%).

Final exam evaluation 70% with Lab works, or 100% for those that didn't make lab work.

6. COHERENCE BETWEEN TEACHING METHODOLOGIES AND OBJECTIVES

This course consists of the presentation of several circuits or systems, in theoretical lectures and interactive lessons. To design arithmetic circuits, it is necessary for students to understand some typical circuits, as with the design of sequential circuits. Problem solving in the classroom allows students to train and acquire these skills. The study of memory begins with a lecture of their internal constitution which allows the student to understand and subsequently project the expansion of those memories. The same applies to the study of the controllers. The

analogue to digital conversion also requires lectures, problem solving and hardware assembly.

The classes with laboratory work serve to the experimental validation of theories.

7. ATTENDANCE

Cabinet 64, at Thursday from 18h 30m to 20 h. Contact - amrmartins@ipg.pt.

DATE

14 October 2023

SIGNATURES

Professor(s), Area/Group Coordinator or Head of Department signatures

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